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(54) Phase difference measuring apparatus and mass flowmeter thereof

(57) A phase difference measuring apparatus for accurately measuring the phase difference (fine time difference) of two signals with the same frequency with a reduced number of bits for A/D conversion is disclosed. In addition to output signals of an upstream side pickup and a downstream side pickup of a mass flowmeter, an output signal of an adding circuit in which the output signals of the upstream side pickup and the downstream side pickup are added is supplied to a comparator, a PLL circuit, an antialias filter, a sample and hold circuit, and

an A/D converter. These circuits quantize these signals and send the quantized signals to a band pass filter. The band pass filter extracts a predetermined signal component and outputs it to a DFT. The DFT performs complex Fourier transformation on the input signal. Thus, the phase difference between two signals with the same frequency (such as an upstream side pickup signal and a downstream side pickup signal) can be accurately detected with a reduced number of bits for each of the A/D converters.

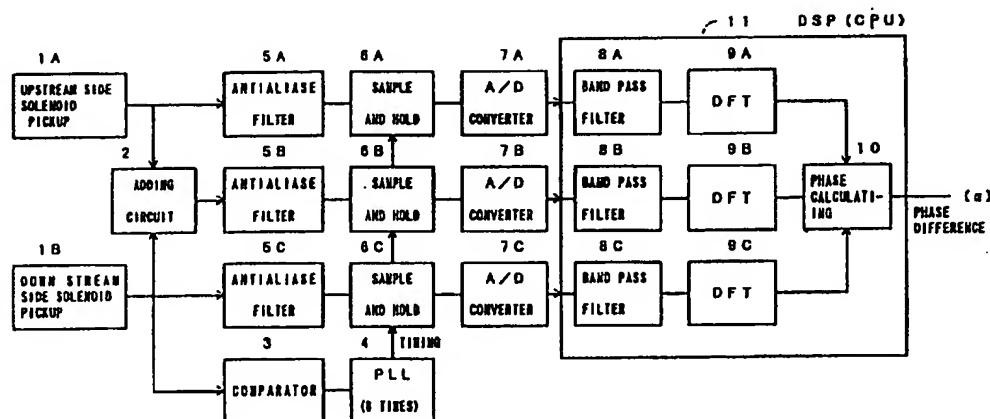


FIG. 10

EP 0 702 212 A2

Description

Background of the Invention

5 Field of the Invention

The present invention relates to a phase difference measuring apparatus for measuring the phase difference between two signals with the same frequency.

10 In addition, the present invention relates to a phase difference measuring apparatus for measuring the phase difference between two signals at a predetermined frequency, in particular, to a modification of an error compensating method in the measurement of the phase difference.

Description of the Related Art

15 Such a phase difference measuring apparatus can be used in various fields. An example of the apparatus is an industrial instrument such as a Coriolis type mass flowmeter that detects the phase difference (time difference) of vibrations due to Coriolis force caused by the mass and speed of a fluid that flows in an upstream side pipe and a downstream side pipe, so as to obtain a flow rate thereof.

Fig. 1 is a schematic diagram showing a primal construction of a Coriolis type mass flowmeter.

20 In Fig. 1, reference numeral 101 is a U shaped pipe in which a fluid flows. At a center portion of the U shaped pipe 101, a permanent magnet 102 is securely disposed. Both edges of the U shaped pipe 101 are secured to a base 103. Reference numeral 104 is a solenoid coil that surrounds the U shaped pipe 101. Reference numeral 105 is a support frame that supports the solenoid coil 104. The frame 105 is securely disposed on the base 103. A base side portion of the U shaped pipe 101 functions as a nodal point of vibration such as a turning fork, thereby preventing vibration energy from being easily lost. Reference numerals 1A and 1B are solenoid pickups that detect velocity of both legs of the U shaped pipe 101. When the U shaped pipe 101 is vibrated at its natural frequency ($\sin \omega t$) by the electromagnetic force that works between the solenoid coil 104 and the permanent magnet 102 secured to the U shaped pipe 101, Coriolis force works on the fluid that flows in the U pipe 101.

Fig. 2 is an isometric view showing a vibration of the U shaped pipe.

30 The magnitude of the Coriolis force is proportional to the mass and speed of the fluid that flows in the U shaped pipe. The direction of the Coriolis force accords with the product of the vectors of the moving direction of the fluid and the angular velocity of the U shaped pipe 101. In addition, since the flow direction of the fluid on the input side of the U shaped pipe 101 is the reverse of that on the output side, Coriolis force that works at both legs of the U shaped pipe 101 produces a twisting torque. This torque varies with the excitation frequency. The amplitude of the torque is proportional to the mass and flow rate of the fluid that flows in the U shaped pipe 101. Fig. 3 is an isometric view showing a vibration mode caused by the twisting torque.

When the amplitude of the twisting torque is detected by the pickups 1A and 1B, the mass and flow rate of the fluid can be obtained. However, the real vibration of the U shaped pipe is the sum of the vibration caused by the solenoid coil 104 and the vibration caused by the twisting torque due to the Coriolis force. The vibration on the upstream side of the U shaped pipe 101 is expressed by $\sin(\omega t - \alpha)$, whereas the vibration on the downstream side thereof is expressed by $\sin(\omega t + \alpha)$. Thus, there is a phase difference (2α), or time difference (Δt) between signals e1 and e2 detected by the pickups 1A and 1B, as shown in Fig. 4. The phase difference varies depending on the type of the pipe and the excitation frequency. In the case of the U shaped pipe 101, when the resonance frequency thereof is 80 Hz, there is a time difference of approximately 120 μs at the maximum flow rate. A resolution of 0.01 % of the maximum phase difference should be compensated. Thus, a time measuring resolution of 12 ns is required.

45 The time difference can be measured by various methods. One of the simplest methods is a method for counting time difference gate pulses using a reference clock. An example of this method is shown in Fig. 5. In Fig. 5, an upstream side pickup signal Pu and a downstream side pickup signal Pd are amplified by respective amplifiers 111 (with an amplification factor of B). The amplified signals are supplied to respective comparators 112. The comparators 112 digitise respective input signals and output digitised signals to an exclusive-OR circuit 113. The exclusive-OR circuit 113 performs an exclusive-OR operation for the digitized signal and outputs a gate pulse Pg with a pulse width that is equivalent to the time difference between the upstream side pickup signal Pu and the downstream side pickup signal Pd. The gate pulse Pg is supplied to a counter 114. The counter 114 measures gate pulse time by counting a reference clock 115 within gate pulse. The frequency of the reference clock should be 85 MHz or higher.

50 When this U shaped pipe is used in a real plant, since it is bent, it has problems of pressure loss and difficulty of cleaning. To solve such problems, a straight-pipe type Coriolis flowmeter has been proposed. Fig. 6 shows an example of the straight-pipe type Coriolis flowmeter.

In Fig. 6, reference numeral 121 is a straight pipe in which a fluid to be measured flows. At a center portion of the straight pipe 121, a permanent magnet 123 is securely disposed. Both edges of the straight pipe 121 are secured to a

base 120. Reference numeral 122 is a solenoid coil that surrounds the straight pipe 121. Reference numeral 124 is a support frame that supports the solenoid coil 122. The frame 124 is secured to the base 120. Since the straight pipe has a higher rigidity and a higher twisting resistance than the U shaped pipe, the time difference between the upstream side pickup signal and the downstream side pickup signal becomes smaller.

5 For example, the resonance frequency of the straight pipe is approximately 1 kHz and the time difference at the maximum flow rate is approximately 2 μ s. The measurement should be performed with a resolution of 0.01 % of the maximum time difference. Thus, a time measuring resolution of 0.2 ns is required. To count pulses, a reference clock with a frequency of 5 GHz is required. It is impossible to produce such a clock oscillator. Even if such a clock oscillator can be produced, when comparators that obtain time difference signals from pickup signals are used, and since jitter
10 due to intermediate zone of input signals takes place (the intermediate zone is an instable level between "1" and "0"), it is doubtful of being able to obtain an accuracy of 0.2 ns.

Thus, the measurement is performed as shown in Fig. 7. The following subtraction between the upstream side pickup signal Pu and the downstream side pickup signal Pd is performed by a differential device (subtracting device) 131.

$$15 \quad \sin(\omega t + \alpha) - \sin(\omega t - \alpha) = 2 \cos \omega t \times \sin \alpha$$

Thus, a weak phase signal with an amplitude of $\sin \alpha$ (where α is 0.1 ns against a period of 1 ms) is obtained. The phase signal is supplied to an amplifier 132 (with an amplification factor of B). The amplified signal is supplied to a narrow band filter 133. The narrow band filter 133 extracts only a predetermined frequency component. The resultant signal is supplied
20 to a full-wave rectifying and detecting device 134. The full-wave rectifying and detecting device 134 outputs a DC level of $B \sin \alpha$. The resultant signal is supplied to an A/D converter 135. The A/D converter 135 outputs a digital value of $\sin \alpha$. Thus, the phase difference α is obtained. Due to the offset current of the amplifier and voltage drift caused temperature, if the temperature environment of the plant is not stable, the measurement error becomes large. Consequently, in practice, the accuracy of 0.01 % of the maximum flow rate cannot be obtained.

25 To prevent the influence of voltage drift in the amplifier, a method for obtaining the phase difference by Fourier transformation of digital signals has been proposed. Fig. 8 is a block diagram showing the construction of an apparatus corresponding to such a method.

Referring to Fig. 8, an upstream side pickup signal Pu and a downstream side pickup signal Pd are obtained by an upstream side pickup 1A and a downstream side pickup 1B, respectively. The upstream side pickup signal Pu and the
30 downstream side pickup signal Pd are supplied to respective amplifiers 141. The amplifiers 141 amplify the upstream side pickup signal Pu and the downstream side pickup signal Pd. The amplified signals are supplied to respective sample and hold circuits 142. The sample and hold circuits 142 sample and hold the amplified signals. The sampled levels are supplied to respective A/D converters 143. The A/D converter 143 digitizes the sampled levels. The resultant digital signals are stored in a data memory 144. The data memory 144 stores the digital signal as a discrete data sequence.
35 A digital signal processor (DSP) 145 performs a digital filtering operation on the discrete data sequence so as to remove a noise component. In addition, the DSP 145 analyzes frequencies of the input signal, and performs a complex Fourier transformation for obtaining a real part and an imaginary part of the signal at exiting frequency, so as to obtain the phases of the real part and imaginary part of the excitation frequency of the solenoid coil.

Next, the theory of phase measurement corresponding to the complex Fourier transformation will be described.

40 Assuming that the Fourier transformation of a time function $f(t)$ is denoted by $F(U)$, $F(U)$ can be expressed by the following equation (1).

$$45 \quad F(U) = \int_{-\infty}^{+\infty} f(t) e^{-jUt} dt \quad (1)$$

50

55

Next, assuming that the Fourier transformation of a time function $f(t + a)$ is $F(U')$, $F(U)$ can be expressed by the following equation (2).

$$F(U') = \int_{-\infty}^{+\infty} f(t + a) e^{-j\omega t} dt$$

$$\text{when } t + a = T$$

$$= \int_{-\infty}^{+\infty} f(T) e^{-j\omega T} e^{j\omega a} dT = e^{j\omega a} \underbrace{\int_{-\infty}^{+\infty} f(T) e^{-j\omega T} dT}_{F(U)}$$

$$= F(U) e^{j\omega a} \dots (2)$$

Figs. 9A and 9B are schematic diagrams showing the relationship between $F(U)$ and $F(U')$. Thus, it is clear that the advance of a phase on the time axis is the advance of a phase in the frequency range. Consequently, assuming

$$F(U) = A + jB,$$

thus,

$$F(U') = F(U) e^{j\omega a} = (A + jB) (\cos \omega a + j \sin \omega a)$$

From these vector components, the phase can be obtained.

In the above-described phase calculation, since the resolution of the vector components affects the resolution of the phase, each of the A/D converters for the pickup signals requires a large number of bits. In addition, the phase detection sensitivity depends on the number of bits of the A/D converters. For example, assuming that the excitation frequency of a straight pipe is 1 kHz and the minimum detectable time is 0.1 ns, the number of bits required for both A/D converters is 24.

Although 24-bit type A/D converters are available, the conversion speed is 16 ms, which is too slow to sample a pickup signal with a frequency of 1 kHz. Moreover, in the case that the full scale of the A/D converter is 10 V, LSB (Least significant bit) is 0.6 μ V. In a plant with a bad noise environment since the error indication becomes large, such the conversion level cannot be smaller. Actually, in practice, the time difference cannot be measured with a resolution of 0.1 ns.

In the case of the straight-pipe type Coriolis flowmeter that has a low pressure loss and easy-cleaning construction, when the method for obtaining the time difference corresponding to the complex Fourier transformation of the digital signal process is used, since the practical detecting resolution is low (approximately, 5 ns), an accuracy of 1 % cannot be accomplished.

As a method for compensating an error in measuring a time difference, one of two signals to be measured is manually connect to two input terminals of a phase difference measuring portion so as to use it as a compensation signal. The measurement value of the phase difference measuring portion is used as an offset value. During the measurement, the offset value is subtracted from the measurement value so as to compensate the measurement value.

However, when measuring a phase difference with high accuracy, variations of the frequency, amplitude, and DC level of a measured signal make errors. Thus, the reference phase difference used for the compensation should be measured with the frequency, amplitude, and DC level that do not vary. Conventionally, a reference phase difference (compensation signal) with no phase difference is generated with one signal. Thus, when the phase difference of signals whose frequencies and amplitudes vary from time to time is measured, the reference phase difference should be manually designated to 0. Since the reference phase difference is generated with the same signal, the same amplitude and the same DC level cannot be used for the two measurement signals, resulting in an error. In addition, when the phase difference deviates significantly from 0°, a satisfactory accuracy cannot be accomplished with the reference of phase difference = 0.

Summary of the Invention

An object of the present invention is to provide a phase difference measuring apparatus with a high detecting resolution so as to obtain a phase difference with high accuracy.

Another object of the present invention is to provide a phase difference measuring apparatus for compensating a phase difference measurement error so as to obtain a high measurement accuracy regardless of variations in frequency, amplitude, and DC level of a measurement signal.

A further object of the present invention is to provide a mass flowmeter with high detecting resolution so as to obtain a phase difference with high accuracy and also to accurately measure a flow rate.

A first aspect of the present invention is a phase difference measuring apparatus for measuring the phase difference of two signals with the same frequency, comprising a calculating means for calculating the sum or the difference of the two signals, a quantizing means for quantizing the output signal of the calculating means and the two signals, a band pass filter means for extracting only a predetermined frequency component from the quantized signals, and a phase difference calculating means for performing a Fourier transformation and a predetermined operation for the output signal of the band pass filter means so as to calculate the phase difference of the signals at a measuring frequency.

As a second aspect of the present invention, the quantizing means of the first aspect includes a comparator for digitizing the amplitude of one of the two signals, a PLL circuit for generating a signal with a frequency n times ($n \geq 2$) higher than the frequency of the output signal of the comparator, and an A/D converting means for quantizing the output signal of the calculating means and the two signals at a timing of the output signal of the PLL circuit.

As a third aspect of the present invention, the calculating means of the first aspect has a gain selecting function for selecting a detection range and a resolution at a timing of the phase difference to be detected.

As a fourth aspect of the present invention, the quantizing means of the first or second aspect includes a sample and hold means for sampling and holding the two signals and the output signal of the calculating means.

A fifth aspect of the present invention is the phase difference measuring apparatus of the first or second aspect, further comprising an amplitude varying means for varying the amplitude of at least one of the two signals, and a compensating means for obtaining compensation data corresponding to the variation of the amplitudes of the two signals and for compensating the phase difference corresponding to the compensation data.

A sixth aspect of the present invention is the phase difference measuring apparatus of the first or second aspect further comprising a signal amplitude difference detecting means for detecting the amplitude difference of the two signals, and a gain control amplifier for matching the amplitude of one of the two signals with the amplitude of the other signal corresponding to the amplitude difference.

According to the present invention, in addition to two signals with the same frequency, a third signal that is generated by adding the former two signals or by subtracting one of the two signals from the other signal is used. The amplitudes and phases of the three signals are used. Thus, the number of bits required for each A/D converter can be smaller than for the conventional method that uses the two signals. In addition, the phase difference of the two signals can be accurately detected. Consequently, to obtain an accuracy of 0.01 %, the number of bits required for each of the A/D converters is as small as 14 to 16 bits.

In addition, since the comparator that digitizes the amplitudes of one of the two signals with the same frequency and the PLL circuit that generates a signal with a frequency that is n times higher than the frequency of the output signal of the comparator ($n \geq 2$), the cut-off frequency of each digital filter can be varied corresponding to the variation of the signal frequencies without need to change constants of the program used for the digital filter calculations.

When the calculating means that obtains the sum or the difference of the two signals has the gain selecting function, the detecting range and resolution of the phase difference to be detected can be varied. When the quantizing means has the sample hold means that samples and holds the two signals and the output signal of the calculating means, these signals can be accurately measured.

When the amplitude varying means that varies the amplitudes of the two signals and the compensating means that compensates the phase difference thereof are additionally used, the phase difference can be accurately obtained regardless of the difference in the amplitudes of the two signals. Alternatively, when the signal amplitude difference detecting means that detects the difference in the amplitudes of the two signals and the gain control amplifier that matches the

amplitudes of the two signals corresponding to the detected amplitude difference are used, the same effect can be obtained.

A seventh aspect of the present invention is a phase difference measuring apparatus for measuring the phase difference of two signals at a predetermined frequency, comprising a compensation signal generating means for generating a compensation signal for designating at least one kind of a phase difference with the same frequency as the frequency of one of two measurement signals, a selecting means for selecting the measurement signals and the compensation signal, a phase difference measuring means for measuring the phase difference of each of the measurement signals and the compensation signal, and a compensation control means for controlling the selecting means so as to compensate the measurement value supplied from the phase difference measuring means.

As an eighth aspect of the present invention, the compensation signal generating means of the seventh aspect includes a digitizing means for digitizing one of the two measurement signals, a frequency multiplying means for multiplying the frequency of the digitised signal by a predetermined value, an address generating means for generating addresses which cycle in accord with one cycle of the measurement signal corresponding to the output signal of the frequency multiplying means, at least one storage means for prestoring data that represents one cycle of a sine wave with the addresses that are output from the address generating means, and two D/A converters for converting the sine wave data that is output from the storage means into an analog signal.

A ninth aspect of the present invention is the phase difference measuring apparatus of the seventh or eighth aspect, further comprising first and second amplitude detecting means for detecting the amplitudes of the two measurement signals, third and fourth amplitude detecting means for detecting the amplitudes of the two compensation signals, a first comparing means for comparing the output signal of the first amplitude detecting means with the output signal of the third amplitude detecting means, a second comparing means for comparing the output signal of the second amplitude detecting means with the output signal of the fourth amplitude detecting means, and a pair of amplitude control means for matching the amplitude of each of the measurement signals with the amplitude of each of the compensation signals corresponding to the compared results.

A tenth aspect of the present invention is the phase difference measuring apparatus of the seventh or eighth aspect, further comprising first and second DC level detecting means for detecting the DC levels of the two measurement signals, third and fourth DC level detecting means for detecting the DC levels of the two compensation signals, a first comparing means for comparing the output signal of the first DC level detecting means with the output signal of the third DC level detecting means, a second comparing means for comparing the output signal of the second DC level detecting means with the output signal of the fourth DC level detecting means, and a pair of DC level control means for matching the DC level of each of the measurement signals with the DC level of each of the compensation signals.

An eleventh aspect of the present invention is the phase difference measuring apparatus of the eighth aspect, further comprising a shifting means for shifting the addresses generated by the address generating means, and a designating means for controlling a shift amount and generating at least one type of a phase difference signal.

A twelfth aspect of the present invention is the phase difference measuring apparatus of the seventh, further comprising a notifying means for notifying the compensation control means of the input of a reference signal to the phase difference measuring means, a storage means for storing the measurement value of the phase difference measuring means corresponding to the input from the notifying means, and an adjusting means for obtaining the difference between the stored value and the measurement value of the phase difference measuring means and for canceling the phase difference of the reference signal corresponding to the difference.

A thirteenth aspect of the present invention is a phase difference measuring apparatus for measuring the phase difference of two signals at a predetermined frequency, comprising a clock generating means for generating a digital clock with a predetermined frequency, an address generating means for generating cyclic addresses corresponding to the clock, a shifting means for shifting the addresses generated by the address generating means, at least one pair of storage means for prestoring data that represents one cycle of a sine wave with the cyclic addresses generated by the address generating means and the shift means, two D/A converters for converting sine wave data that is output from the storage means into analog signals, a selecting means for selecting the measurement signals and the output signals of the D/A converters, a frequency detecting means for detecting the frequency of one of the two measurement signals, two amplitude detecting means for detecting the amplitudes of the two measurement signals, two DC level detecting means for detecting the DC levels of the two measurement signals, and a compensation control means for premeasuring the relationship of frequencies, amplitudes, DC levels, and a phase difference of output signals of the D/A converters, obtaining compensation data therefrom, storing the compensation data, and search (look up) or interpolating the compensation data from conditions of frequencies, amplitudes, DC levels, and phase differences that are adjacent to the conditions of the measurement signals.

According to the present invention, the compensation signal source with the same frequency, the same amplitude, and the same DC level as those of two measurement signals is disposed in the compensation unit of the phase difference measuring unit. Alternatively, the compensation signal source has the same frequency, the same amplitude, or the same DC level as those of the two measurement signals and the phase difference is known. As the seventh aspect of the present invention, the compensation signal and the measurement signal are measured on a time-sharing basis. Alter-

natively, as the thirteenth aspect of the present invention, the measurement signal is compensated corresponding to the compensation data that is stored as the compensation signal. Thus, an error due to the variation of at least one of the frequency, amplitude, and DC level can be compensated for.

In addition, according to the eighth aspect or eleventh aspect of the present invention, the phase difference of the compensation signals can be freely designated. Moreover, according to the nineteenth aspect of the present invention, the amplitude (AC level) of the measurement signal can be matched with that of the compensation signal. Alternatively, according to the tenth aspect of the present invention, the DC level of the measurement signal can be matched with that of the compensation signal. In addition, according to the twelfth aspect of the present invention, the offset adjustment can be performed.

A fourteenth aspect of the present invention is a mass flowmeter for causing a fluid to flow in a vibrating pipe, and for Coriolis force of the flow and angular vibration of the pipe, to twist-vibrate the pipe, and for obtaining the mass and flow rate of the fluid corresponding to the time difference of the twisted asymmetrical vibrations of the pipe, comprising a pair of detectors for detecting the asynchronous twisting vibrations of the pipe, a calculating means for calculating the sum or the difference of the output signals of the detectors, a quantizing means for quantizing the output signals of the calculating means and the detectors, a band pass filter means for extracting only a predetermined frequency component from the quantized signals, and a phase difference calculating means for performing a Fourier transformation and a predetermined operation on the output signal of the band pass filter means so as to calculate the phase difference of the signals at a measuring frequency.

As a fifteenth aspect of the present invention, the quantizing means of the fourteenth aspect includes a comparator for digitizing the amplitudes of the output signals of the detectors, a PLL circuit for generating a signal with a frequency n times (where $n \geq 2$) higher than the frequency of the output signal of the comparator, a sample and hold means for sampling and holding the output signals of the calculating means and the detectors at a timing of the output signal of the PLL circuit, and an A/D converting means for quantizing the output signal of the sample and hold means.

A sixteenth aspect of the present invention is the mass flowmeter of the fourteenth or fifteenth aspect, further comprising an amplitude varying means for varying the amplitude of at least one of the output signals of the detectors, and a compensating means for obtaining compensation data corresponding to the variation of the amplitudes of the output signals of the detectors and for compensating the phase difference corresponding to the compensation data.

A seventeenth aspect of the present invention is the mass flowmeter of the fourteenth or fifteenth aspect, further comprising a signal amplitude difference detecting means for detecting the amplitude difference in the output signals of the detectors, and a gain control amplifier for matching the amplitude of one of the output signals of the detectors with the amplitude of the other signal corresponding to the amplitude difference.

According to the present invention, along with the upstream side pickup signal and the downstream side pickup signal, a third signal that is obtained by adding the former two signals or subtracting one of these signals from the other signal is used. Since the amplitudes and phases of these three signals are used, the number of bits required for each A/D converter is smaller than that of the conventional method that uses only the upstream side pickup signal and the downstream side pickup signal. In addition, the phase difference between the upstream side pickup signal and the downstream side pickup signal can be accurately detected. Thus, to obtain an accuracy of 0.01 % (a resolution of 0.2 ns) at the maximum flow rate, the number of bits required for each A/D converter is as small as 14 to 16 bits.

In addition, since the comparator that digitizes the signal amplitudes of the two signals with the same frequency and the PLL circuit that generates a signal with a frequency that is n times higher than the frequency of the output signal of the comparator (where $n \geq 2$), the cut-off frequency of each digital filter can be varied corresponding to the variation of the signal frequencies without the need to change constants of the program used for the digital filter calculations. When the amplitude varying means that varies the amplitudes of the upstream side pickup signal and the downstream pickup signal and the compensating means that compensates the phase difference thereof are additionally used, the phase difference can be accurately obtained regardless of the difference in the amplitudes of the upstream side pickup signal and the downstream side pickup signals. Alternatively, when the signal amplitude difference detecting means that detects the difference in the amplitudes of the upstream side pickup signal and the downstream side pickup signal and the gain control amplifier that matches the amplitudes of the two signals corresponding to the detected amplitude difference, the same effect can be obtained.

These and other objects, features and advantages of the present invention will become more apparent in light of the following detailed description of best mode embodiments thereof, as illustrated in the accompanying drawings.

Brief Description of the Drawings

Fig. 1 is a schematic view showing a primal construction of a U shaped pipe type Coriolis mass flowmeter;
 Fig. 2 is a isometric view for explaining a vibration of a U shaped pipe;
 Fig. 3 is a isometric view for explaining a vibration mode caused by a twisting torque of a Coriolis force on the U shaped pipe;

Fig. 4 is a schematic diagram showing an example of pickup signals in the case that a Coriolis force takes place in the U shaped pipe;

Fig. 5 is a block diagram showing a phase difference detecting circuit corresponding to a counter method;

Fig. 6 is a schematic diagram showing a construction of an example of a straight-pipe type Coriolis mass flowmeter;

Fig. 7 is a block diagram showing a phase difference detecting circuit corresponding to a differential amplifying method;

Fig. 8 is a block diagram showing a phase difference detecting circuit corresponding to a direct Fourier transformation method;

Fig. 9A is a schematic diagram for explaining the phase difference detecting theory of complex Fourier transformation, and shows a vector with a frequency of ω in FFT for a waveform with a phase difference of 0;

Fig. 9B is a schematic diagram for explaining the phase difference detecting theory of complex Fourier transformation, and shows a vector with a frequency of ω in FFT for a waveform with a phase difference of ω ;

Fig. 10 is a block diagram showing a first embodiment of the present invention;

Fig. 11 is a vector diagram for explaining the operation of the first embodiment;

Fig. 12 is a block diagram showing a second embodiment of the present invention;

Fig. 13 is a block diagram showing a third embodiment of the present invention;

Fig. 14 is a block diagram showing a fourth embodiment of the present invention;

Fig. 15 is a flow chart showing a process of a compensation control apparatus of Fig. 14;

Fig. 16 is a graph showing an operation of the compensation control apparatus of Fig. 14;

Fig. 17 is a block diagram showing a fifth embodiment of the present invention; and

Fig. 18 is a block diagram showing a sixth embodiment of the present invention.

Detailed Description of the Preferred Embodiments

Fig. 10 is a block diagram showing an embodiment of the present invention. In Fig. 10, reference numerals 1A and 1B are an upstream side solenoid pickup and a downstream side solenoid pickup, respectively. Reference numeral 2 is an adding circuit. Reference numeral 3 is a comparator. Reference numeral 4 is a phase lock loop (PLL). Reference numerals 5A, 5B, and 5C are antialias filters. Reference numerals 6A, 6B, and 6C are sample and hold circuits. Reference numerals 7A, 7B, and 7C are A/D converters. Reference numerals 8A, 8B, and 8C are band pass filters. Reference numerals 9A, 9B, and 9C are Discrete Fourier Transformers (DFTs). Reference numeral 10 is a phase calculating portion. The band pass filters 8A, 8B, and 8C, the DFTs 9A, 9B, and 9C, the phase calculating portion 10, and so forth are programmed in a digital signal processor (DSP) 11.

The upstream side pickup 1A outputs a signal $A \sin(\omega t - \alpha)$. The downstream side pickup 1B outputs a signal $-B \sin(\omega t + \alpha)$. Thus, when the adding circuit 2 shown in Fig. 10 is used, the connection of the upstream side pickup 1A is the reverse of the connection of the downstream side pickup 1B, so that the phase difference between the upstream side pickup signal and the downstream side pickup signal becomes 180 deg at a flow rate of 0 ($\alpha = 0$). When a subtracting circuit is used, it is not necessary to connect the upstream side solenoid pickup 1A and the downstream side solenoid pickup 1B in reverse.

The output signal of the adding circuit 2 can be expressed by the following equation (3).

$$A \sin(\omega t - \alpha) - B \sin(\omega t + \alpha) = -2A \sin \alpha \cos \omega t + (A - B) \sin(\omega t + \alpha) \quad (3)$$

At this point, the output signal of the adding circuit 2 that has a gain selecting function can be expressed by the following equation.

$$k\{-2A \sin \alpha \cos \omega t + (A - B) \sin(\omega t + \alpha)\}$$

When the constant k is variable, the resolution of the A/D converter 7B can be varied. In addition, the phase difference detecting resolution can be varied.

Assuming that the upstream side pickup signal is vector A, the downstream side pickup signal is vector B, and the output signal of the adding circuit is vector C these vectors can be represented as shown in Fig. 11. When the flow rate is 0 ($\alpha = 0$), the direction of the vector A does not accord with the direction of the x-axis ($\sin \omega t$) in Fig. 11 due to delays of the circuit system, the start position of a waveform used for discrete Fourier transformation, and so forth.

Assuming that the deviation angle is θd , the angle between the vector A and the delay axis of the circuit reference is θa , and the angle between the vector B and the delay axis of the circuit reference is θb , the angle θd can be expressed by the following equation (4).

$$(\theta a - \theta d) + (\theta b - \theta d) = \pi \quad (4)$$

$$\theta d = (\theta a + \theta b - \pi) / 2$$

Thus, the angle θe of the vector C to the x-axis can be expressed by the following equation (5).

$$\theta e = \theta c - \theta d = \theta c - (\theta a + \theta b - \pi) / 2 \quad (5)$$

On the other hand, the component of the y-axis of the vector C can be expressed by the following equation (6).

$$C \sin \theta e = 2A \sin \alpha - (A - B) \sin \alpha \quad (6)$$

Thus, assuming that the phase difference between the upstream side and the downstream side is α , the phase difference α can be expressed by the following equation (7).

$$\alpha = \sin^{-1} [C \sin \{\theta c - (\theta a + \theta b - \pi) / 2\} / (A + B)] \quad (7)$$

The equation (7) represents that α , that is proportional to the mass and flow rate, can be obtained from the amplitudes and phases of the vectors A, B, and C. Since the sine function of the equation (7) is "1" in the normal state ($A=B$), α can be obtained from the magnitude (amplitude) of each vector. Thus, this method is easier than the conventional method in which the phase difference is obtained using only the vectors A and B. Consequently, according to this method, the number of bits required for each A/D converter can be reduced.

When the amplitudes and phases of the three signals are obtained, in this embodiment, these signals are supplied to low pass filters (LPF) 5A, 5B, and 5C in fig 10 (these filters are referred to as antialiasing filters) so as to remove noise components. The output signals of the LPFs 5A, 5B, and 5C are supplied to sample and hold circuits 6A, 6B, and 6C, respectively. The sample and hold circuits 6A, 6B, and 6C sample and hold respective input signals. The sampling timings of the sample and hold circuits 6A, 6B, and 6C are generated by the, comparator 3 and the PLL 4. In this embodiment, the sampling frequency is eight times higher than the measuring frequency.

To reproduce the original signal, the input signal should be sampled with a frequency that is two or more times higher than the frequency of the original signal. Thus, in this case, the PLL 4 functions as a frequency multiplier. In addition, to improve the detecting accuracy of the phase difference, many A/D converter bits (for example, 16 bits) are required. In this embodiment, the comparator 3 and the PLL 4 are disposed on the downstream pickup 1B side. However, it should be noted that the comparator 3 and the PLL 4 can be disposed on the upstream pickup 1A side.

The output signals of the sample and hold circuits 6A, 6B, and 6C are supplied to the A/D converters 7A, 7B, and 7C, respectively. The A/D converters 7A, 7B, and 7C digitize the respective input signals. The digitized signals are supplied to the band pass filters 8A, 8B, and 8C. The band pass filters 8A, 8B, and 8C extract respective measuring frequencies. The resultant signals are supplied to the DFTs 9A, 9B, and 9C. The DFTs 9A, 9B, and 9C obtain the amplitudes and phases of the measuring frequencies. The DFTs 9A, 9B, and 9C are used to obtain the amplitudes and phases of predetermined frequency components at high speed. Thus, to obtain all frequency components, FFTs (Fast Fourier Transformers) can be used instead of the DFTs. The phase calculating portion 10 calculates the equation (7) for the output signals of the DFTs 9A, 9B, and 9C and thereby obtains α .

The band pass filters 8A, 8B, and 8C work on data that has been sampled at a frequency eight times higher than the measuring frequency. However, even if the measuring frequency varies corresponding to the density of the fluid, the sampling frequency correspondingly varies so as to follow the pass bands of the band pass filters. Thus, it is not necessary to change filter constants and so forth of the program.

Thus, α can be accurately obtained. However, α is adversely affected by the difference in delays of the digitizing circuits for the three signals and the delay of the adding circuit. As an example of this influence, when there is an amplitude difference between the upstream side and the downstream side, α calculated by the equation (7) varies. (When the amplitude difference is constant, since it is treated as a constant offset, it can be simply compensated.) To prevent such an influence, the following two methods can be used in practice.

(1) Method for intentionally changing the amplitude difference between the upstream side, and the downstream side and correspondingly obtaining a compensation coefficient (according to a second embodiment of the present invention):

When the amplitude difference between the upstream side and the downstream side varies, α of the equation (7) varies. This is because the "sin" angle of the equation (7) contains a constant error, due mainly to the delay of the adding circuit 2. Thus, as shown in Fig. 12, when variable gain amplifiers (gain control amplifiers) 12A and 12B are adjusted, and thereby there is an amplitude difference between the upstream side and the downstream side, a phase compensating portion 13 compensates the phase difference of an output signal θc of the adding circuit 2 through a DFT 9B (namely, the phase compensating portion 13 advances the phase of the output signal θc) so that the delay of the adding circuit 2 is removed.

To obtain a coefficient to be used for such a compensation (to advance the phase of the program), when the phase difference between the upstream side and the downstream side is constant, a phase compensation data searching algorithm 14 varies the gains of the variable gain amplifiers 12A and 12B. Thus, the amplitude on the upstream side or the downstream side is intentionally varied and thereby causes a phase difference. The variation of α is recorded. The value of the constant for compensating the phase θ_c is varied so that the variation becomes a minimum. At this point, the variation of amplitudes of the upstream side and the downstream side should be 1 % or less. To perform measurement with an accuracy of 0.01 % at the maximum flow rate, the compensation constant for the phase θ_c should have an accuracy in the range of 0.005 deg to 0.008 deg. In addition, even if the phase difference between the variable gain amplifiers is varied, the phase difference error thereof should be 0.

(2) Method for using gain control amplifiers for keeping the amplitude difference between the upstream side and the downstream side constant (according to a third embodiment of the present invention):

As shown in Fig. 13, variable gain amplifiers 12A and 12B, peak hold portions 15A and 15B that hold peak values of the output signals of the solenoid pickups 1A and 1B, a subtracting circuit 16 that calculates the difference between the peak values, and a low pass filter (LPF) 17 that removes noise corresponding to the difference are disposed after solenoid pickups 1A and 1B.

The variable gain amplifiers 12A and 12B are adjusted corresponding to the difference between the peak values on the upstream side and the downstream side (namely the output signal of the subtracting circuit 16) so as to remove the influence of the amplitude difference between the upstream side and the downstream side. When the gains of the variable gain amplifiers 12A and 12B are varied, it is necessary to prevent a phase difference between the input signals and the output signals thereof. In this embodiment, the gain of the variable gain amplifier 12A is variable, whereas the gain of the variable gain amplifier 12B is fixed. However, it should be noted that this relationship can be reversed.

In the above-mentioned embodiments, the Coriolis type mass flowmeter was described. However, it should be appreciated that the present invention is not limited to only this type of apparatus. Instead, the present invention can be applied to any apparatus that measures the phase difference between two signals with the same frequency.

Fig. 14 is a block diagram showing a fourth embodiment of the present invention.

In Fig. 14, reference numeral 21 is a comparator. Reference numeral 22 is a PLL (phase lock loop) that is a frequency multiplying circuit. Reference numerals 23A to 23D are amplitude detecting circuits. Reference numerals 24A and 24B are DC level detecting circuits. Reference numerals 25A and 25B are DC level comparing circuits. Reference numerals 26A and 26B are signal relays that are selectors. Reference numeral 27 is a phase difference measuring portion. Reference numeral 28 is a compensation control unit. Reference numerals 29A and 29B are amplitude comparison circuits. Reference numerals 30A and 30B are DC level control circuits. Reference numeral 31 is an address generating circuit. Reference numeral 32 is an address shifting circuit. Reference numeral 33 is a fetching timing generating circuit. Reference numerals 34A and 34B are ROMs that are sine tables. Reference numerals 35A and 35B are digital/analog (D/A) converters. Reference numerals 36A and 36B are amplitude control circuits.

In this embodiment, measurement signals 1 and 2 that are sine waves with the same frequency are input. The phase difference between the measurement signals 1 and 2 is obtained. The measurement signal 2 is compared with a mean value of the measurement signal 2 by the comparator 21. The resultant signal of the comparator 21 is supplied to the PLL circuit 22. The PLL circuit 22 multiplies the frequency of the output signal of the comparator 21 by, for example, 16,384. Corresponding to the output signal of the PLL circuit 22, the address generating circuit 31 generates 16,384 addresses per one cycle. Corresponding to these addresses, data is read from the ROMs 34A and 34B.

At this point, sine wave amplitude data, of which one cycle is composed of 16,384 addresses, has been stored in the ROMs 34A and 34B. The amplitude data is composed of all bits combined so as to improve the resolution. (In other words, for eight bits, 0 to 255 are used.) The address shifting circuit 32 shifts the address of the ROM 34A corresponding to the phase difference designating signal received from the compensation control unit 28, so as to mutually move the data of the ROMs 34A and 34B. Thus, data to be referenced in the ROM 34A differs from data to be referenced in the ROM 34B. The designated resolution of the phase difference depends on the multiplication factor of the PLL circuit 22. In this embodiment, the resolution of the phase difference is $360 \text{ deg}/16,384 (= 0.021973 \text{ deg})$.

The ROMs 34A and 34B output digital data that has a phase difference corresponding to the phase difference designating signal to the D/A converters 35A and 35B, respectively. The D/A converters 35A and 35B convert the digital data into analog compensation signals. The output signals of the D/A converters 35A and 35B are synchronized using a fetching timing signal generated by the timing generating circuit 33 corresponding to the output signal of the PLL circuit 22.

Although the output signals of the D/A converters 35A and 35B have a phase difference corresponding to the phase difference designating signal, the amplitudes of the output signals should accord with those of the measurement signal. In this embodiment, the amplitude reference signals of the D/A converters are varied so as to vary the magnitude (for example voltage) per bit. In other words, although the amplitudes are varied, the phase difference of the signals (delay) is not varied.

The amplitude detecting circuits 23A and 23B detect the amplitudes of the measurement signals 1 and 2, respectively. The amplitudes of the output signals of the D/A converters 35A and 35B are detected by the amplitude detecting circuits 23C and 23D, respectively. The output signals of the amplitude detecting circuits 23A and 23C are compared by the amplitude comparison circuit 29A. The output signals of the amplitude detecting circuits 23B and 23D are compared by the amplitude comparison circuit 29B. Thus, amplitude errors between the measurement signals and the output signals of the D/A converters (compensation signals) are obtained. The amplitude control circuits 36A and 36B control the amplitude reference signals (maximum value) of the D/A converters 35A and 35B so as to decrease the errors.

In the above-described method, the amplitudes of the signals (AC components) are matched. Likewise, the centers (or DC levels) of the measurement signals and the output signals (compensation signals) of the D/A converters are matched by the DC level detecting circuits 24A to 24D, the DC level comparing circuits 25A and 25B, the DC level control circuits 30A and 30B, and so forth. The DC levels of the signals are horizontally shifted while the difference between the maximum and the minimum values of the amplitude reference signal for each D/A converter is kept constant.

The output signals of the D/A converters (compensation signals) have the same frequency, the same amplitude, and the same DC level as those of the measurement signals 1 and 2. The phase difference of the output signals of the D/A converters is a known value corresponding to the phase difference designating signal. Thus, with these signals, the phase difference measuring portion 27 is compensated.

Fig. 15 is a flow chart showing the compensation process.

In this compensation process, compensation signals α_1' and α_2' corresponding to phase difference designating signals α_1 and α_2 , and a measurement signal (with a phase difference α'), are alternately measured on a time sharing basis. The selection of these signals is performed by the compensation control unit 28 corresponding to the phase difference designating signal and the relay selecting signal. In this case, the measurement time of the compensation signals (with phase differences of α_1' and α_2') should be sufficiently smaller than the measurement time of the measurement signal (α') within the range that the predetermined compensation accuracy is satisfied, so as to prevent the response to the variation of the phase difference of the measurement signals.

In such a method, the phase differences α_1' , α_2' , and α' are measured. Corresponding to the results, a compensation as shown in Fig. 16 is performed. The phase differences α_1' and α_2' preferably accord with the upper limit and the lower limit of the phase differences, from the point of view of accuracy.

In Fig. 16, the horizontal axis represents measured results α_1' , α_2' , and α' obtained by the phase difference measuring portion 27. The vertical axis represents the designated phase differences α_1 and α_2 and the measured result α that has been compensated. In Fig. 16, with values for α_1' , α_2' , α' , α_1 , and α_2 known, α is obtained. In practice, a straight line that passes through two points (α_1' , α_1) and (α_2' , α_2) is obtained. From the straight line, the value α on the vertical axis corresponding to the value α' on the horizontal axis is obtained. Thus, α is the accurate phase difference between the measurement signals of which a phase difference measurement error due to variations in frequency, amplitude, and DC level, has been compensated for.

In the above-described compensation, although the influence due to errors in the frequency, amplitude, and DC level can be removed, there may still be an offset-type phase difference between the measurement signals 1 and 2. Depending on the application for measuring a phase difference, as the measured results of the measurement signals 1 and 2 that have a phase difference, the phase difference should be 0. In this case, phase difference signals that are input as the measurement signals 1 and 2 are treated as reference 0 signals. The reference 0 signal (zero adjust signal) are input from an input unit to a compensation control unit 28. The compensated data is stored in a non-volatile memory 28A or the like in the compensation control unit 28. The value is subtracted from the compensated data. In this method, offset of phase difference are adjusted (zero adjustment).

In the fourth embodiment, the measurement signals and the compensation signals are alternately selected on a time sharing basis so as to remove error components due to variations in frequency, amplitude, and DC level. However, in an application in which the phase difference of measurement signals sharply varies, the decrease of the response of the time sharing process may adversely affect the measurement result. To solve such a problem, as a fifth embodiment, a set of data used for the compensation has been prepared. Corresponding to the prepared data, the measurement result of the phase difference is compensated. This method is referred to as an offline method. In this method, it takes a long time to obtain the compensation data. In addition, any changes in tolerances with age cannot be compensated for. However, the response of the measurement result virtually does not degrade.

Fig. 17 is a block diagram showing a fifth embodiment of the present invention.

In this embodiment, the frequency of a compensation signal is designated by the oscillation frequency (OSC) of a crystal oscillator 41, the ratio (N/M) of frequency dividers 42A and 42B, and the number of clock pulses (CYC) which is necessary for one cycle of a sine wave that is output from each D/A converter. Thus, the frequency of the compensation signal is expressed by the following equation.

$$f = \text{OSC} \times (N / M) / (\text{CYC})$$

The control method of the amplitudes, DC levels, and phase differences of the compensation signals of this embodiment is the same as those of the fourth embodiment. However, in the fifth embodiment, the amplitudes and DC levels are controlled by a compensation control unit 28, unlike for those of the fourth embodiment.

The compensation control unit 28 has obtained compensation data used for measurement. The compensation data is a four-dimensional table composed of frequencies, amplitudes, DC levels, and phase differences of compensation signals. Thus, as the number of samples of each dimension increases, the data amount of the compensation data remarkably increases. Consequently, the number of samples of each dimension should be reduced. Since the compensation data does not fully accord with the conditions of all measurements, linear interpolation between two adjacent data in each dimension of the compensation data needs to be used so as to improve the compensation accuracy without the need to increase the data amount of the compensation data.

Thus, by subtracting compensation data that is searched (look up) or interpolated from a phase difference measurement value of a phase difference measuring portion 27, errors in frequencies, amplitudes, and DC levels can be compensated for.

The difference between the fourth embodiment and the fifth embodiment is whether or not compensation is performed on a real time basis. In these embodiments, errors due to variations of frequencies, amplitudes, and DC levels are compensated. In a sixth embodiment, only an error due to a variation in frequencies is compensated for. However, the circuit construction can be simplified. This embodiment can be applied for an application in which an error due to a variation in frequencies is dominant, and errors due to variations in amplitudes and DC levels are rare. Fig. 18 is a block diagram showing a construction of the fifth embodiment of the present invention.

One of the measurement signals is connected to the + side input terminal of a differential amplifier 51 with an amplification factor of 1. The - side input terminal of the differential amplifier 51 is grounded. A compensation control unit 28 controls relays 26A and 26B so as to alternately select the measurement signals, and a compensation signal that is output from the differential amplifier 51 on time sharing basis. With reference to a phase difference of 0 deg or 180 deg of the measured result of the compensation signal, the phase difference of the measurement signals is compensated for.

In this embodiment, a differential amplifier 51 is used as a reference signal generator with a phase difference of 180 deg. In addition, a transformer can be used as a reference signal generator with a phase difference of 180 deg. As a reference signal that can be easily generated, one measurement signal is connected to both input terminals of the phase difference measuring portion so as to generate a reference signal with a phase difference of 0 deg. The phase difference of the reference signal can be selected from 0 deg and 180 deg in consideration of a phase difference to be measured, accuracy of the compensation, circuit scale to be added, and so forth. In any case, the magnitude of the variation of the phase difference of reference signals corresponding to the variations of frequencies, amplitudes, and DC levels of the measurement signals, should be sufficiently smaller than the error of the phase difference measuring portion to be compensated.

Although the present invention has been shown and described with respect to best mode embodiments thereof, it should be understood by those skilled in the art that the foregoing and various other changes, omissions, and additions in the form and detail thereof may be made therein without departing from the spirit and scope of the present invention.

Claims

1. A phase difference measuring apparatus for measuring the phase difference between two signals with the same frequency, comprising:
 - calculating means (2) for calculating the sum or the difference of the two signals;
 - quantizing means (3, 4, 6A to 6C, 7A to 7C) for quantizing the output signal of said calculating means (2) and the two signals;
 - band pass filter means (8A to 8C) for extracting only a predetermined frequency component from the quantized signals; and
 - phase difference calculating means (9A to 9C, 10) for performing a Fourier transformation and a predetermined operation on the output signal of said band pass filter means (8A to 8C), so as to calculate the phase difference of the signals at a measuring frequency.
2. The phase difference measuring apparatus as set forth in claim 1,
 - wherein said quantizing means includes:
 - a comparator (3) for digitizing the amplitude of one of the two signals;
 - a PLL circuit (4) for generating a signal with a frequency n times (where $n \geq 2$) higher than the frequency of the output signal of the comparator (3); and
 - A/D converting means (7A to 7C) for quantizing the output signal of said calculating means and the two signals at a timing of the output signal of the PLL circuit.

3. The phase difference measuring apparatus as set forth in claim 1,
wherein said calculating means (2) has a gain selecting function for selecting a detection range and a resolution corresponding to the phase difference to be detected.
- 5 4. The phase difference measuring apparatus as set forth in claim 1,
wherein said quantizing means includes sample and hold means (6A to 6C) for sampling and holding the two signals and the output signal of said calculating means.
- 10 5. The phase difference measuring apparatus as set forth in claim 1, further comprising:
amplitude varying means (12A, 12B) for varying the amplitude of at least one of the two signals; and
compensating means (13) for obtaining compensation data corresponding to the variation in the amplitudes of the two signals and for compensating the phase difference corresponding to the compensation data.
- 15 6. The phase difference measuring apparatus as set forth in claim 1, further comprising:
signal amplitude difference detecting means (15A, 15B, 16) for detecting the amplitude difference of the two signals; and
a gain control amplifier (12A, 12B) for matching the amplitude of one of the two signals with the amplitude of the other signal corresponding to the amplitude difference.
- 20 7. A phase difference measuring apparatus for measuring the phase difference between two signals at a predetermined frequency, comprising:
compensation signal generating means (21, 22, 31, 34A, 34B, 35A, 35B) for generating a compensation signal for designating at least one kind of a phase difference with the same frequency as the frequency of one of two measurement signals;
25 selecting means (26A, 26B) for selecting the measurement signals and the compensation signal;
phase difference measuring means (27) for measuring the phase difference between each of the measurement signals and the compensation signal; and
compensation control means (28) for controlling said selecting means so as to compensate the measurement value supplied from said phase difference measuring means.
- 30 8. The phase difference measuring apparatus as set forth in claim 7,
wherein said compensation signal generating means includes:
digitizing means (21) for digitizing one of the two measurement signals;
frequency multiplying means (22) for multiplying the frequency of the digitized signal by a predetermined
35 value;
address generating means (31) for generating addresses whose cycle accords with one cycle of the measurement signal corresponding to the output signal of said frequency multiplying means;
at least one storage means (34A, 34B) for prestoring data that represents one cycle of a sine wave with the addresses that are output from said address generating means; and
40 two D/A converters (35A, 35B) for converting the sine wave data that is output from said storage means into an analog signal.
- 45 9. The phase difference measuring apparatus as set forth in claim 7, further comprising:
first and second amplitude detecting means (23A, 23B) for detecting the amplitudes of the two measurement signals;
third and fourth amplitude detecting (23C, 23D) means for detecting the amplitudes of the two compensation signals;
first comparing means (29A) for comparing the output signal of said first amplitude detecting means with the output signal of said third amplitude detecting means;
50 second comparing means (29B) for comparing the output signal of said second amplitude detecting means with the output signal of said fourth amplitude detecting means; and
a pair of amplitude control means (36A, 36B) for matching the amplitude of each of the measurement signals with the amplitude of each of the compensation signals corresponding to the compared results.
- 55 10. The phase difference measuring apparatus as set forth in claim 7, further comprising:
first and second DC level detecting means (24A, 24B) for detecting the DC levels of the two measurement signals;
third and fourth DC level detecting means (24C, 24D) for detecting the DC levels of the two compensation signals;

first comparing means (25A) for comparing the output signal of said first DC level detecting means with the output signal of said third DC level detecting means;

second comparing (25B) means for comparing the output signal of said second DC level detecting means with the output signal of said fourth DC level detecting means; and

a pair of DC level control means (30A, 30B) for matching the DC level of each of the measurement signals with the DC level of each of the compensation signals.

11. The phase difference measuring apparatus as set forth in claim 8, further comprising:

shifting means (32) for shifting the addresses generated by said address generating means (31); and
designating means for controlling a shift amount and generating at least one type of a phase difference signal.

12. The phase difference measuring apparatus as set forth in claim 7, further comprising:

notifying means for notifying said compensation control means (28) of the input of a reference signal to said phase difference measuring means (27);

storage means (28A) for storing the measurement value of said phase difference measuring means corresponding to the input from said notifying means; and

adjusting means for obtaining the difference between the stored value and the measurement value of the phase difference measuring means and for canceling the phase difference of the reference signal corresponding to the difference.

13. A phase difference measuring apparatus for measuring the phase difference of two signals at a predetermined frequency, comprising:

clock generating means (41, 42A, 42B, 43, 44) for generating a digital clock signal with a predetermined frequency;

address generating means (31) for generating cyclic addresses corresponding to the clock;

shifting means (32) for shifting the addresses generated by said address generating means;

at least a pair of storage means (34A, 34B) for prestoring data that represents one cycle of a sine wave with the cyclic addresses generated by said address generating means and said shift means;

two D/A converters (35A, 35B) for converting sine wave data that is output from said storage means into analog signals;

selecting means (26A, 26B) for selecting the measurement signals and the output signals of said D/A converters;

frequency detecting means (40) for detecting the frequency of one of the two measurement signals;

two amplitude detecting means (23A, 23B) for detecting the amplitudes of the two measurement signals;

two DC level detecting means (24A, 24B) for detecting the DC levels of the two measurement signals; and

compensation control means (28) for premeasuring the relationship of frequencies, amplitudes, DC levels, and a phase difference of output signals of said D/A converters, obtaining compensation data therefrom, storing the compensation data, and searching or interpolating the compensation data from conditions of frequencies, amplitudes, DC levels, and phase differences that are adjacent to the condition of the measurement signals.

14. A mass flowmeter for causing a fluid to flow in a vibrating pipe and Coriolis force of the flow and angular vibration of the pipe to twist-vibrate the pipe, and for obtaining the mass and flow rate of the fluid corresponding to the time difference between twisted asymmetrical vibrations of the pipe, comprising:

a pair of detectors (1A, 1B) for detecting the asynchronous twisting vibrations of the pipe;

calculating means (2) for calculating the sum or the difference of the output signals of said detectors;

quantizing means (3, 4, 6A to 6C, 7A to 7C) for quantizing the output signals of said calculating means (2)

and said detectors;

band pass filter means (8A to 8C) for extracting only a predetermined frequency component from the quantized signals; and

phase difference calculating means (9A to 9C, 10) for performing a Fourier transformation and a predetermined operation for the output signal of said band pass filter means (8A to 8C) so as to calculate the phase difference of the signals at a measuring frequency.

15. The mass flowmeter as set forth in claim 14,

wherein said quantizing means includes:

a comparator (3) for digitizing the amplitudes of the output signals of the detectors;

a PLL circuit (4) for generating a signal with a frequency n times ($n \geq 2$) higher than the frequency of the output signal of the comparator (3);

sample and hold means (6A to 6C) for sampling and holding the output signals of said calculating means

and said detectors at a timing of the output signal of the PLL circuit; and
A/D converting means (7A to 7C) for quantizing the output signal of the sample and hold means (6A to 6C).

- 5 16. The mass flowmeter as set forth in claim 14, further comprising:
amplitude varying means (12A, 12B) for varying the amplitude of at least one of the output signals of said
detectors (1A, 1B); and
compensating means (13) for obtaining compensation data corresponding to the variation in the amplitudes
of the output signals of said detectors and for compensating the phase difference corresponding to the compensation
data.
- 10 17. The mass flowmeter as set forth in claim 14, further comprising:
signal amplitude difference detecting means (15A, 15B, 16) for detecting the amplitude difference between
the output signals of said detectors; and
a gain control amplifier (12A, 12B) for matching the amplitude of one of the output signals of said detectors
15 with the amplitude of the other signal corresponding to the amplitude difference.
18. A phase difference measuring method for measuring the phase difference between two signals with the same fre-
quency, comprising the steps of:
calculating the sum or the difference of the two signals;
20 quantizing the calculated signals and the two signals;
extracting only a predetermined frequency component from the quantized signals; and
performing a Fourier transformation and a predetermined operation on the extracted signal, so as to calculate
the phase difference of the signals at a measuring frequency.

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FIG. 1

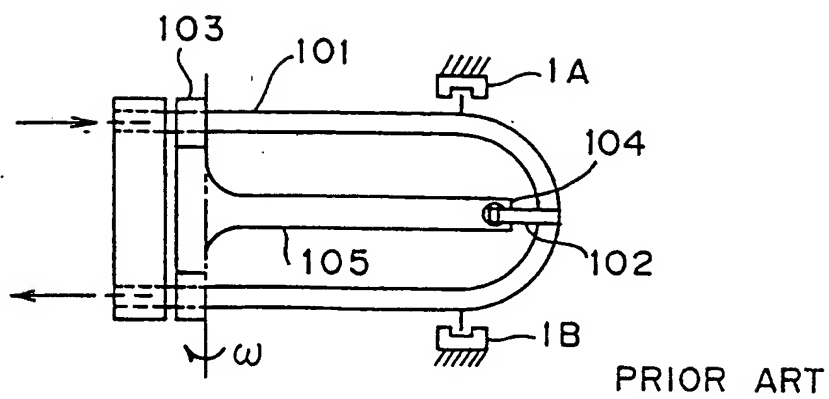


FIG. 2

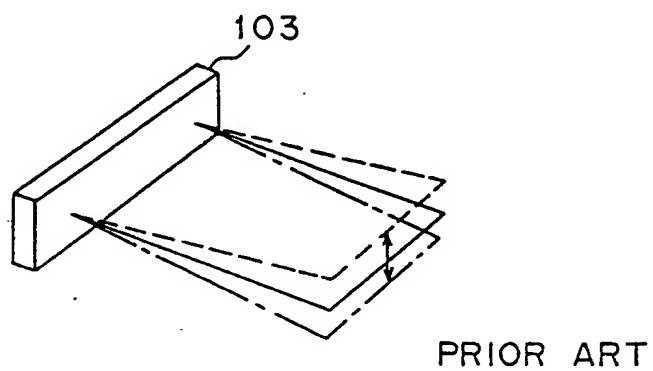
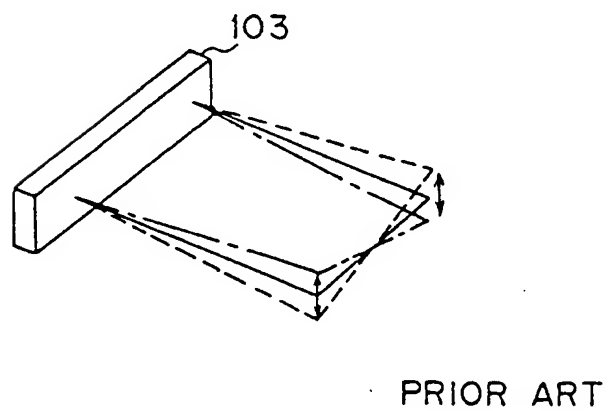


FIG. 3



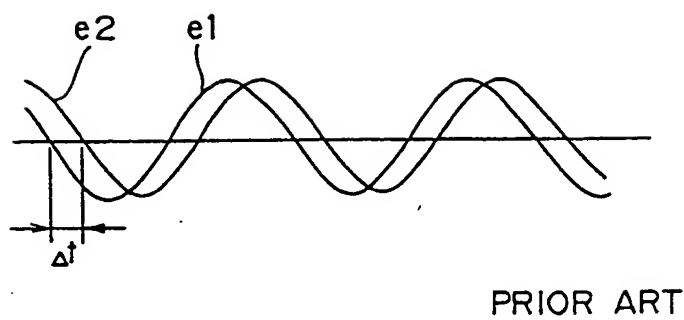


FIG. 4

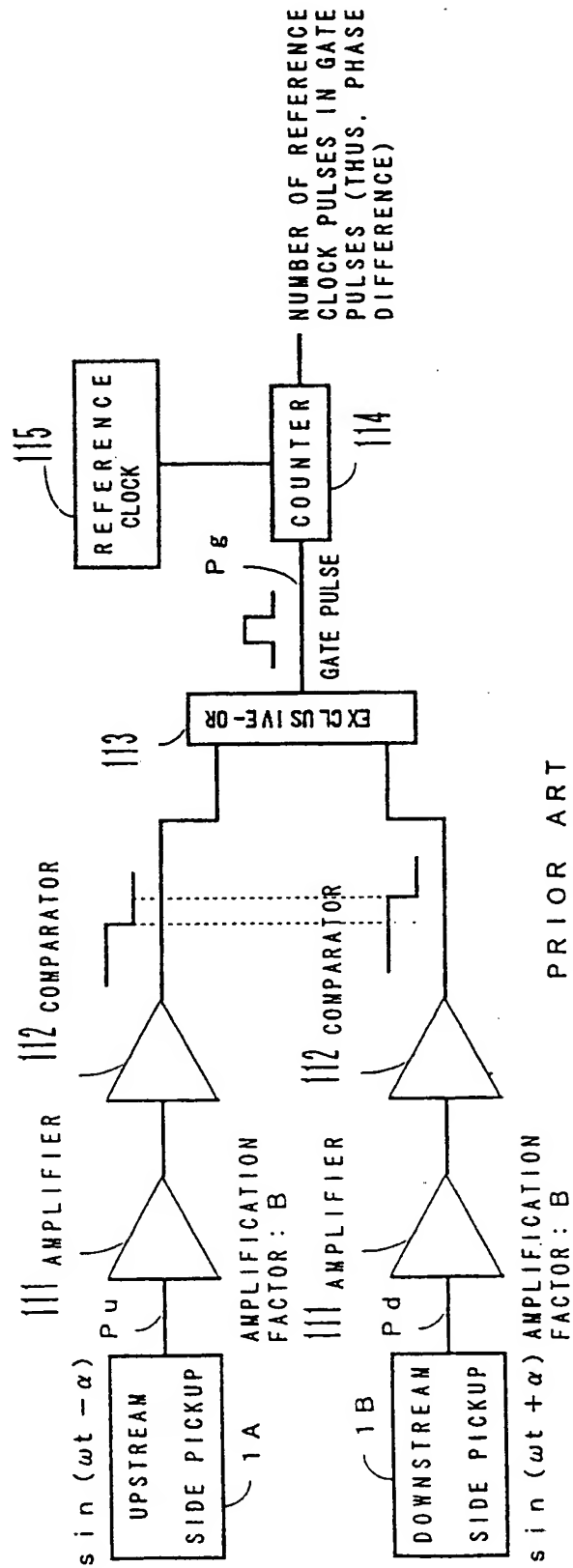
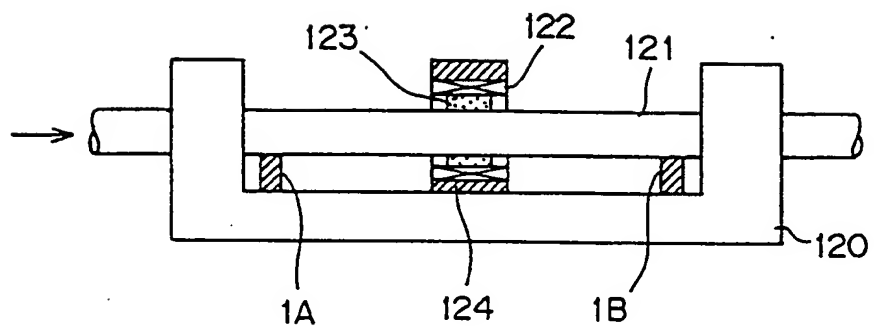


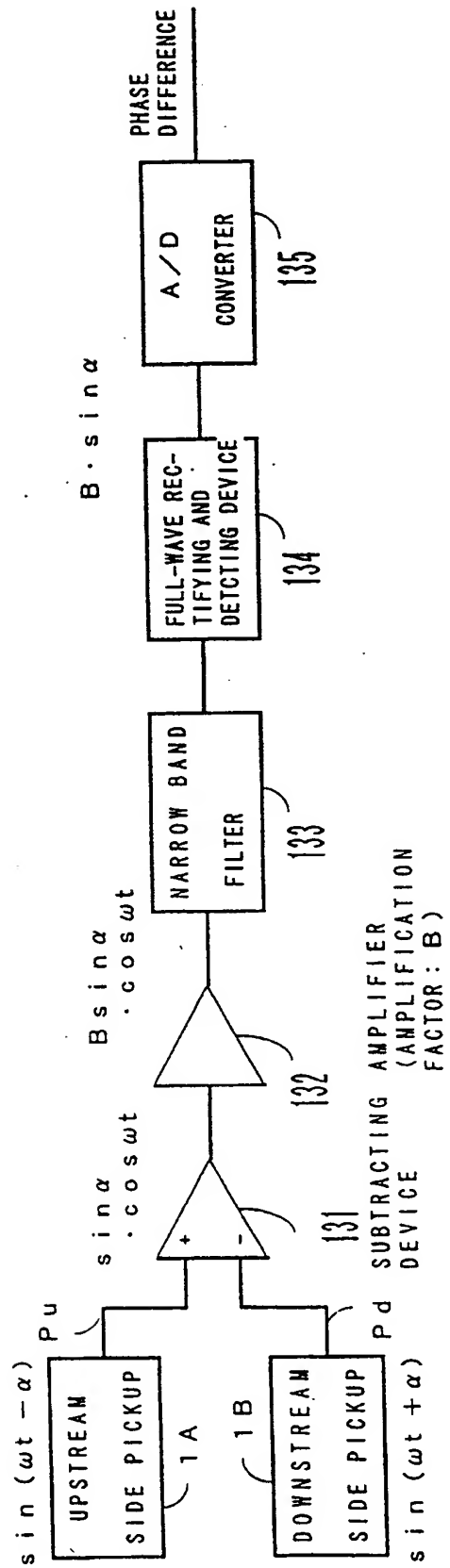
FIG. 5

PRIOR ART



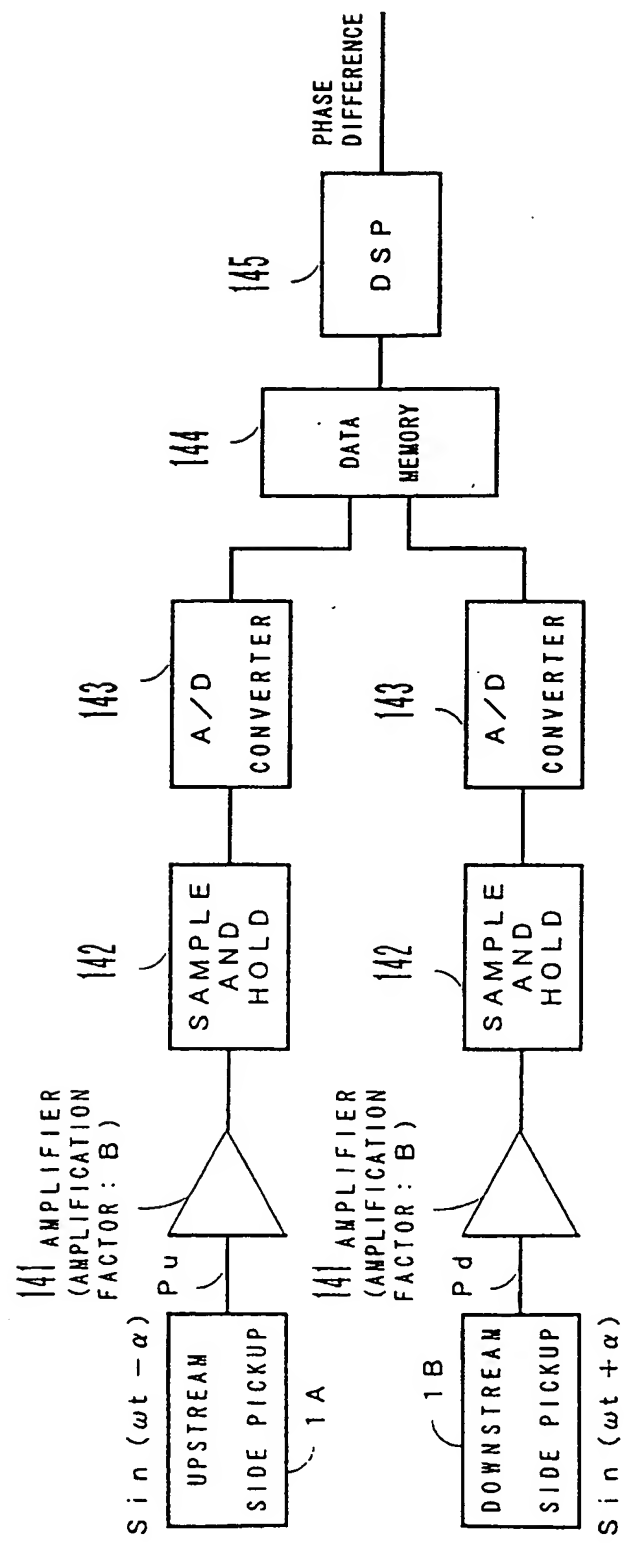
PRIOR ART

FIG. 6



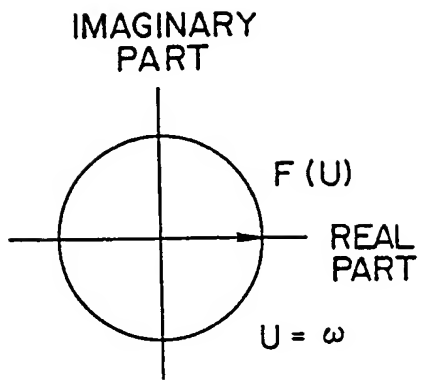
PRIOR ART

FIG. 7



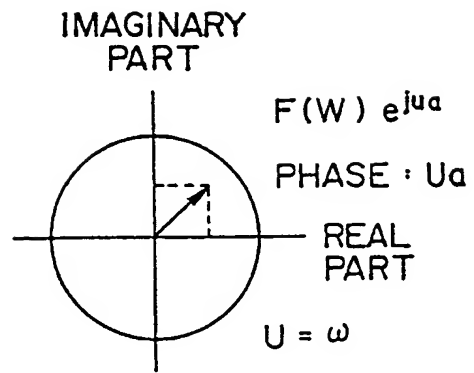
PRIOR ART

FIG. 8



PRIOR ART

FIG. 9A



PRIOR ART

FIG. 9B

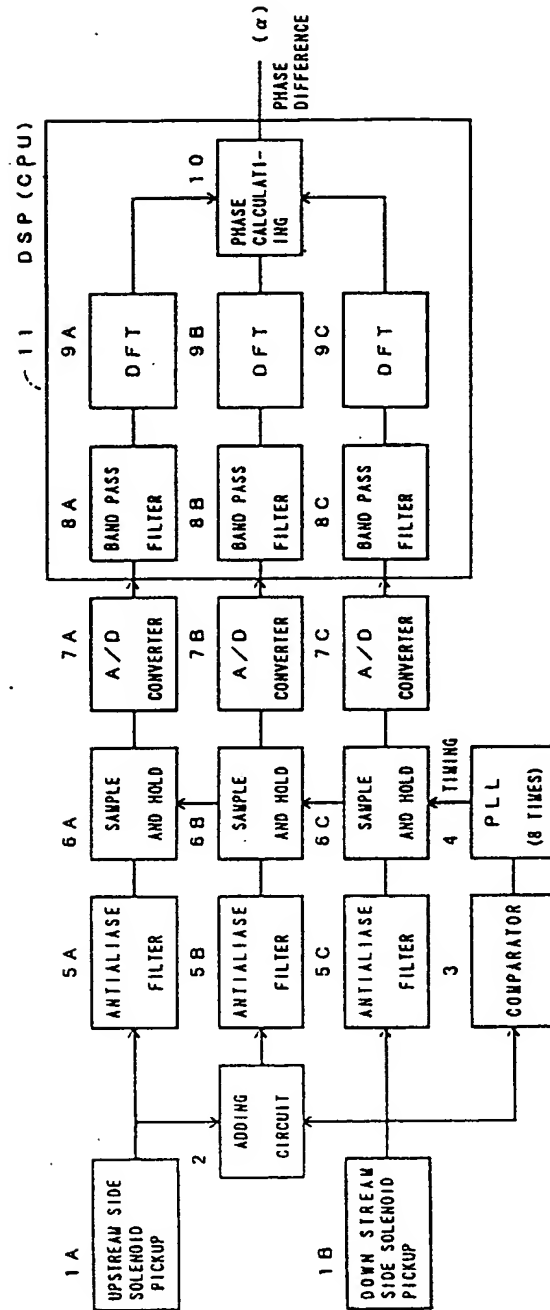


FIG. 10

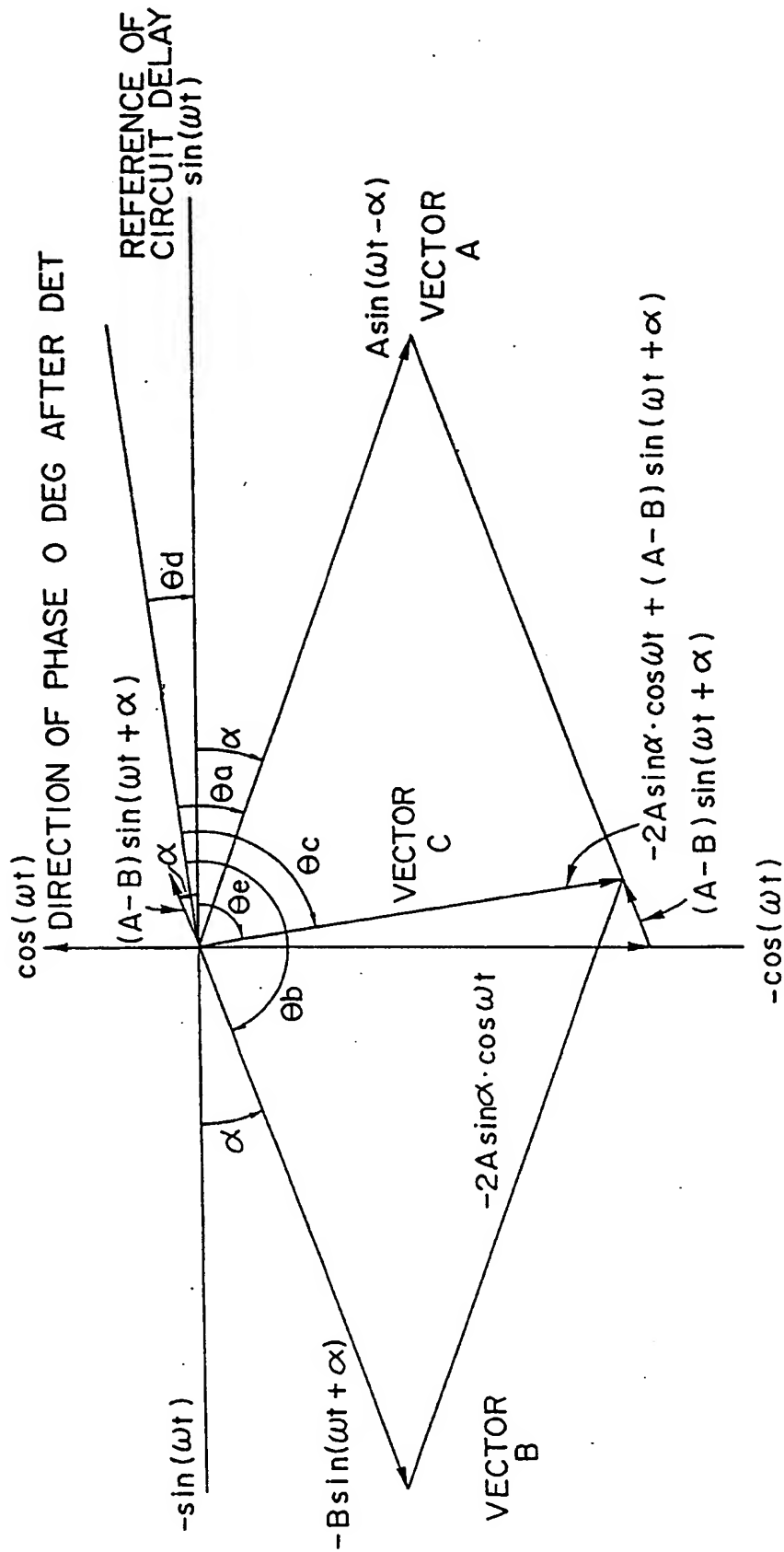


FIG. 11

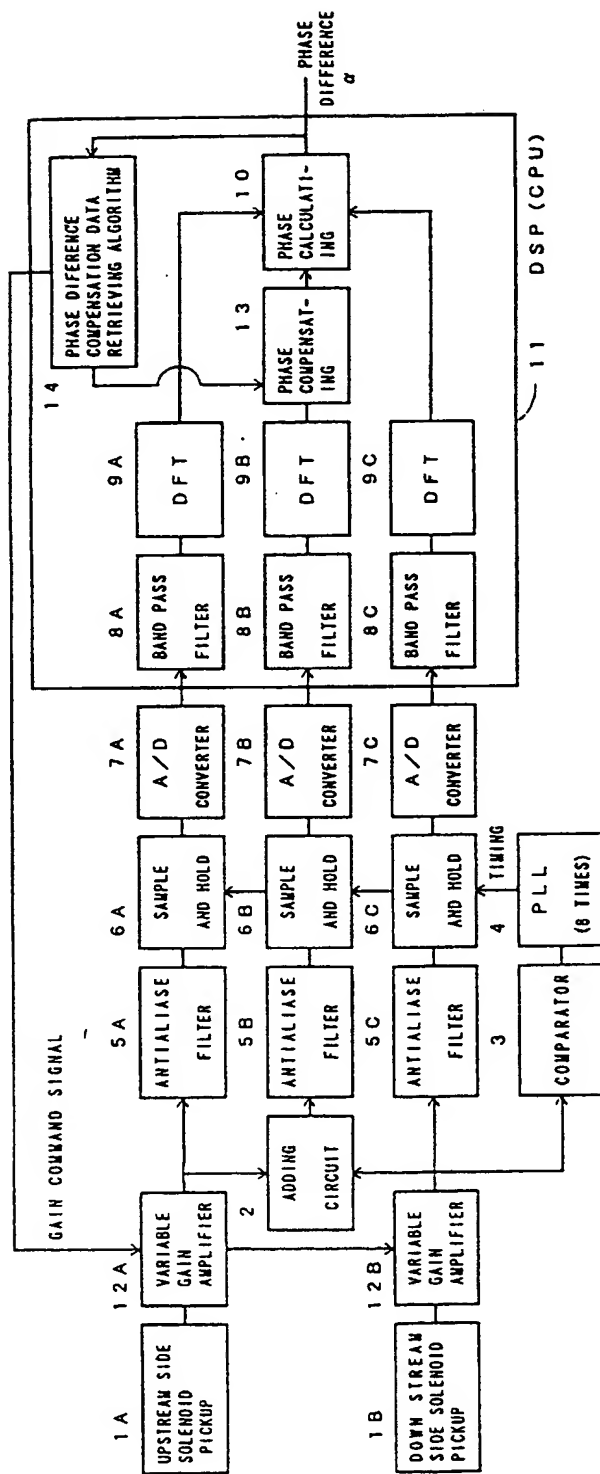


FIG. 12

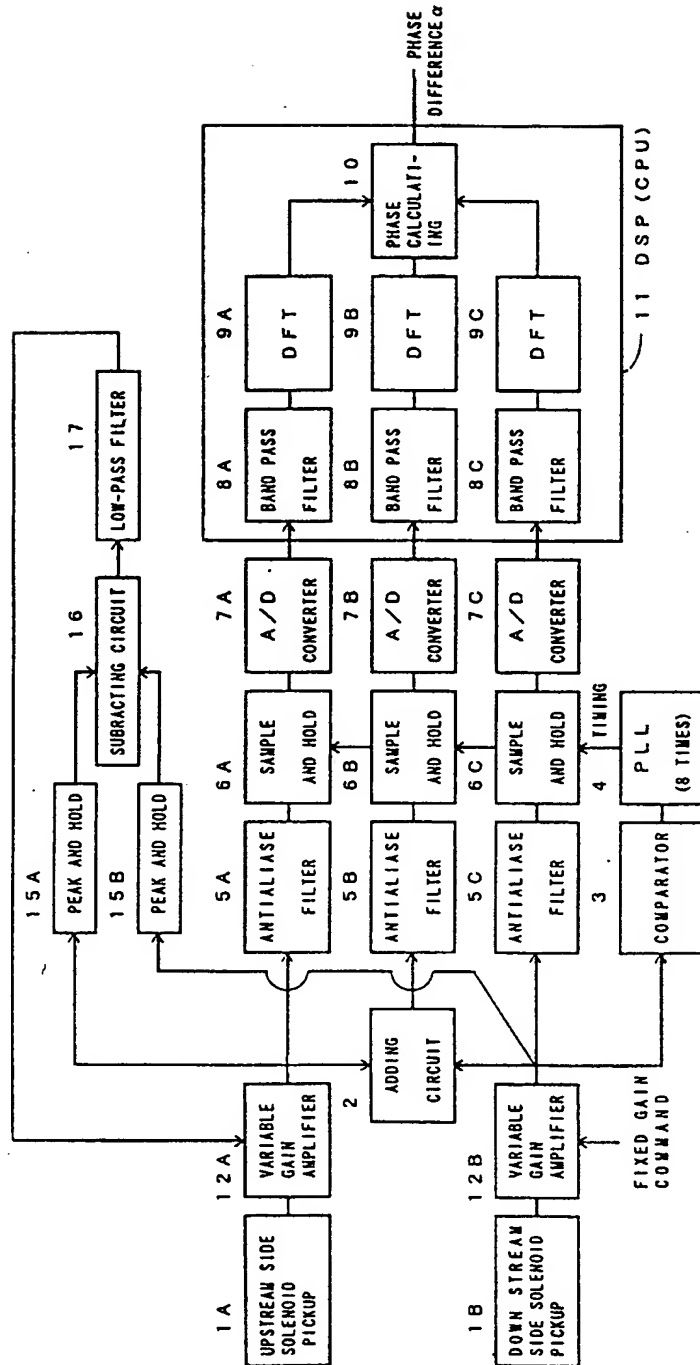


FIG. 13

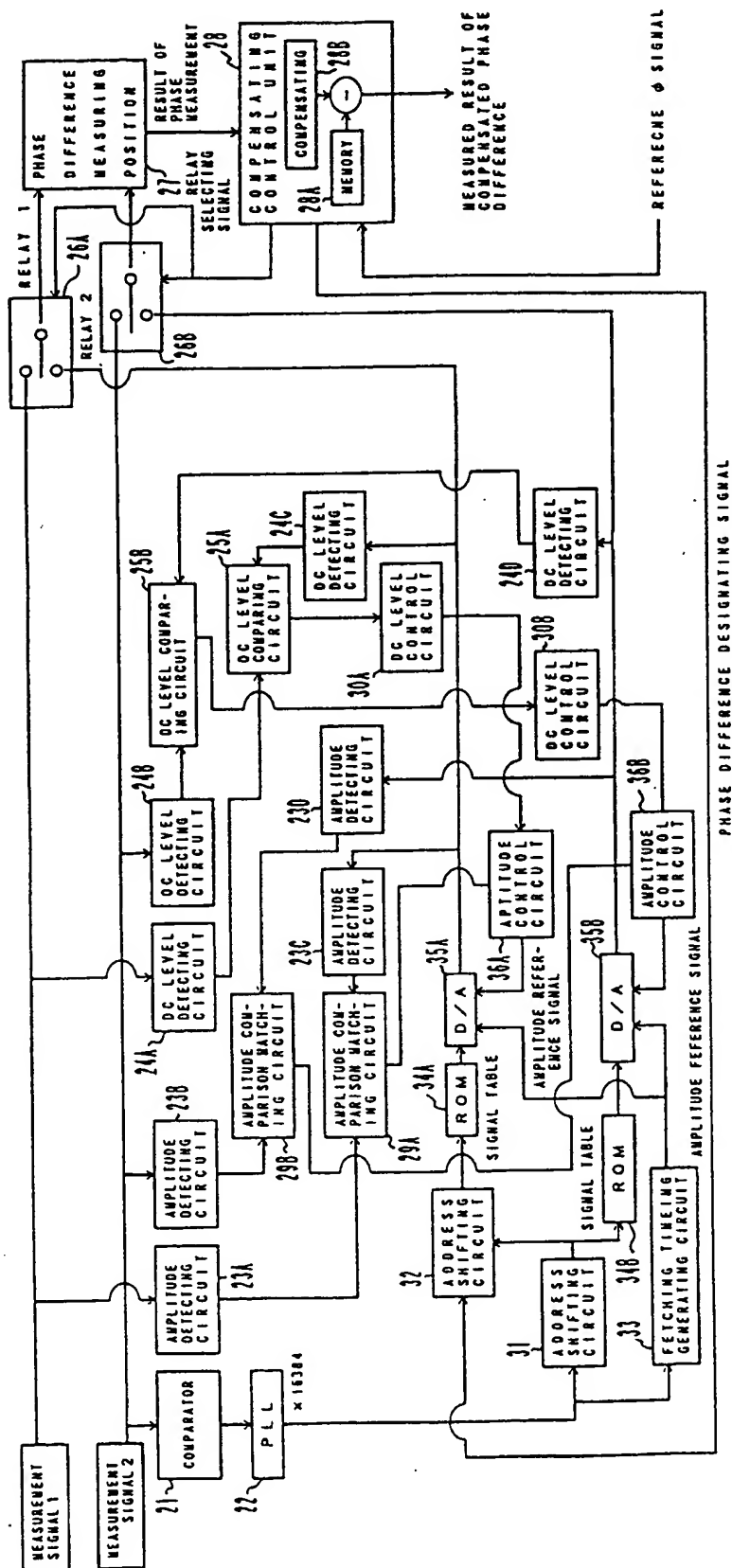


FIG. 14

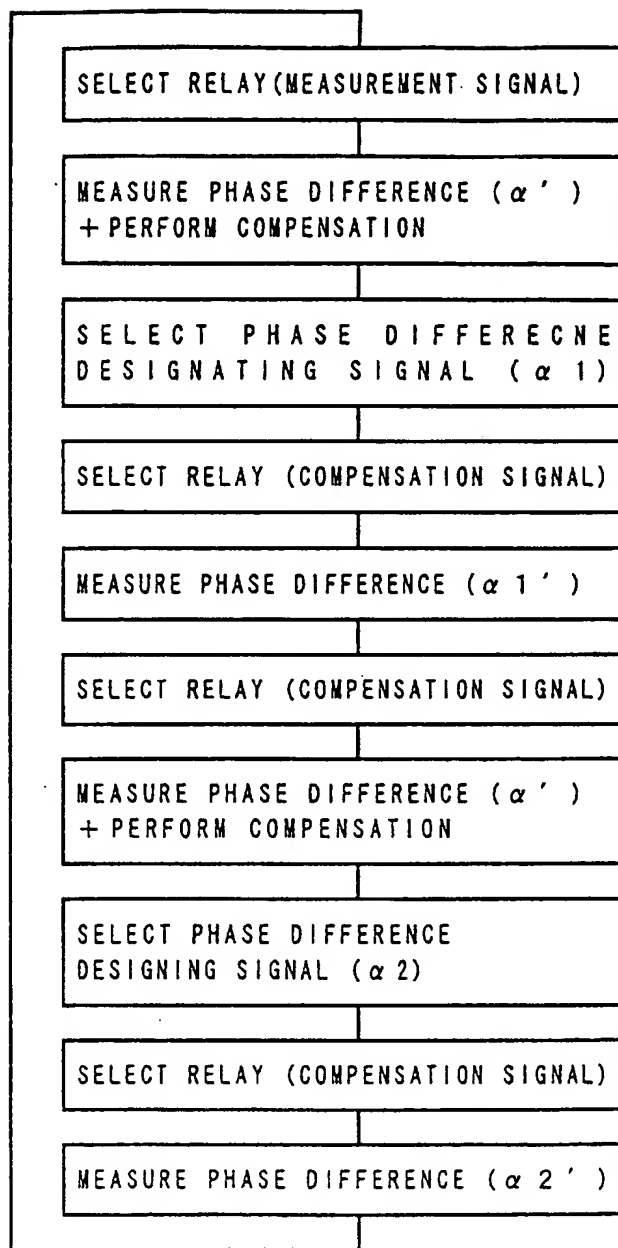


FIG. 15

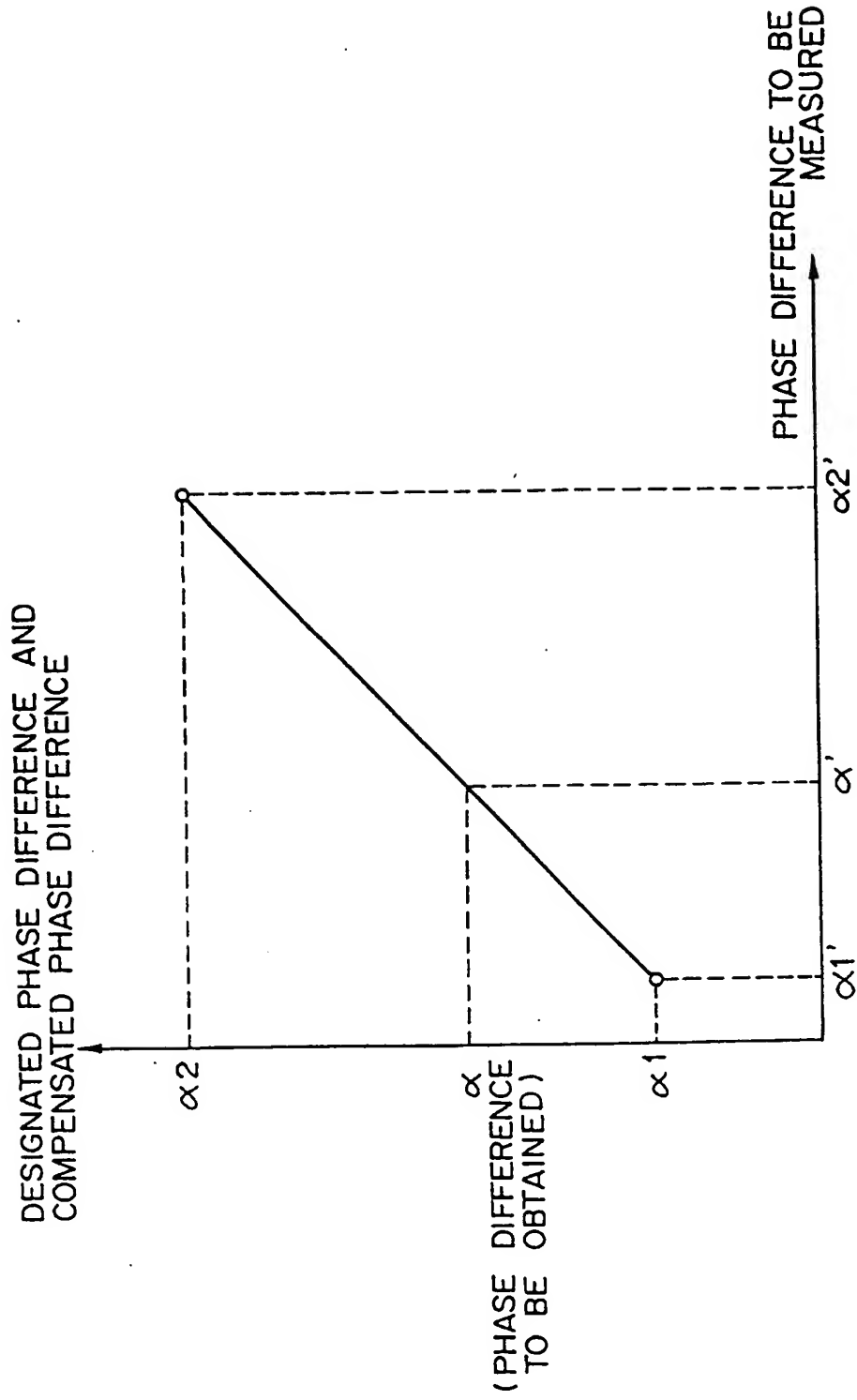


FIG. 16

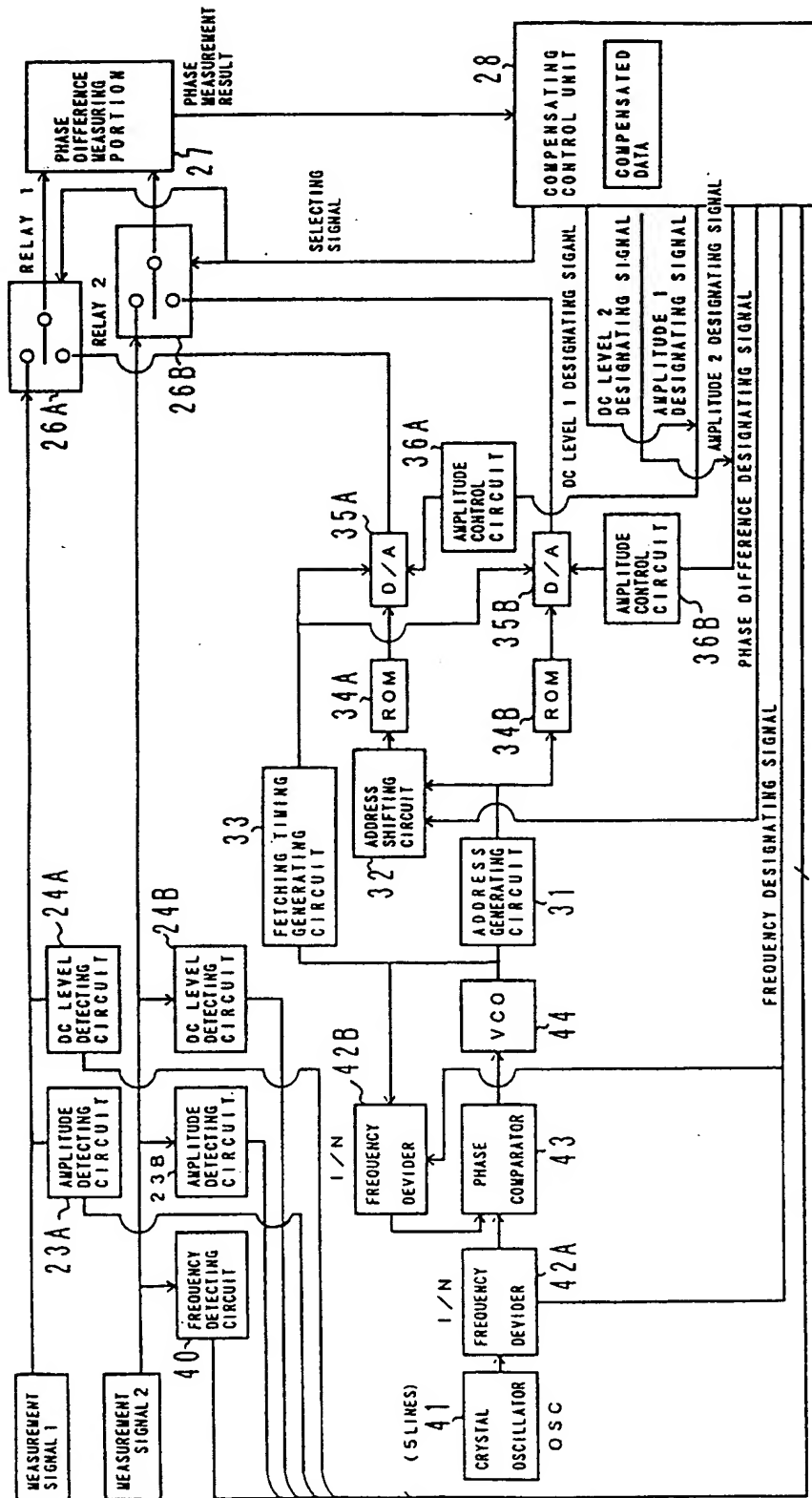


FIG. 17

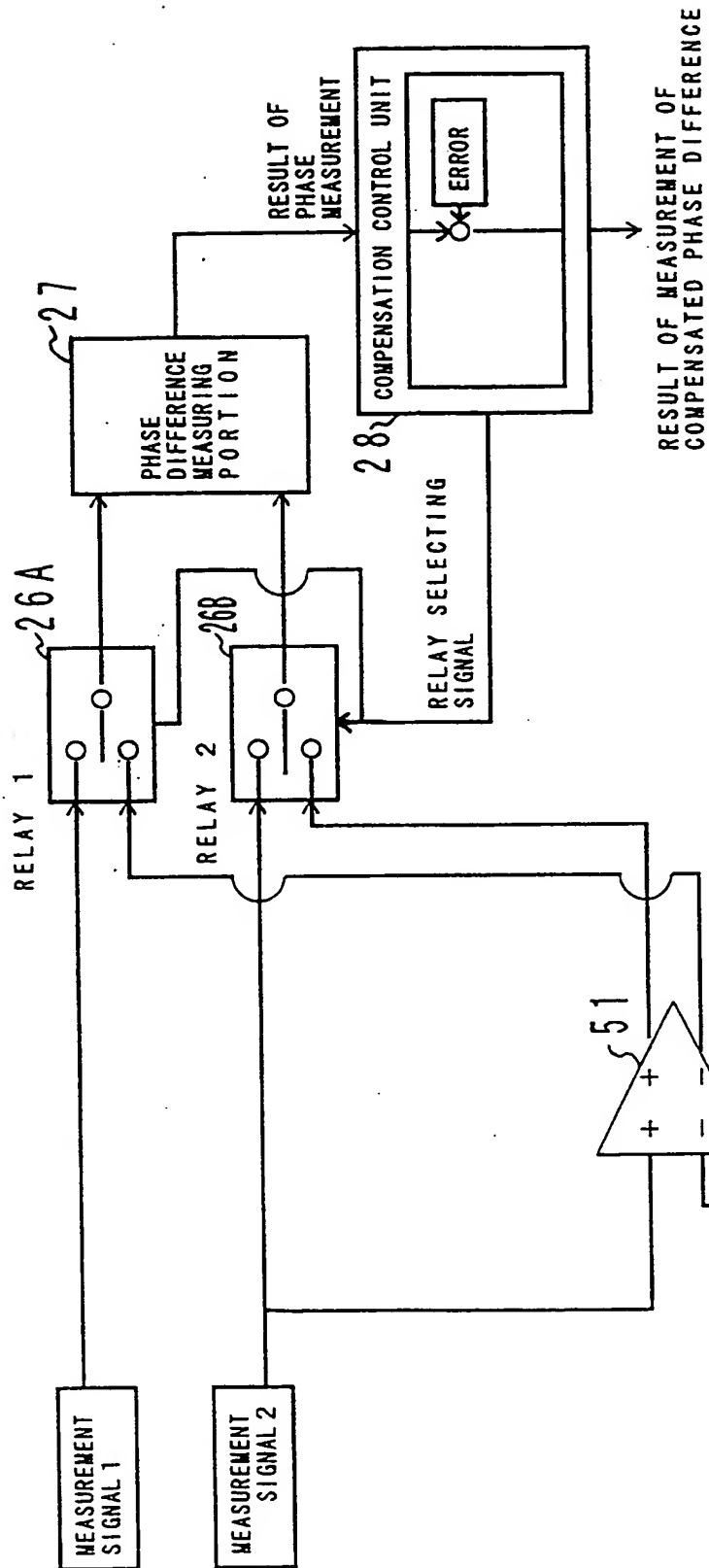


FIG. 18

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